In the Claims:

1. (Currently amended) A data link layer processor comprising:

one or more media access controllers (MACs) for receiving a frame from a communication network; ~~and~~

each of said one or more MACs includes a MAC preprocessor and a MAC postprocessor; and

a statistics acquisition module, operatively coupled to the one or more MACs, for compiling statistics associated with each of the plurality of MACs.

2. (Currently amended) A switching device comprising:

one or more physical layer interfaces for receiving one or more frames from a communication network;

a plurality of data link layer processors, wherein each data link layer processor comprises:

one or more media access controllers (MACs), wherein each MAC is operatively coupled to a physical layer interface, each of said one or more MACs includes a MAC preporcessor and a MAC postprocessor; and

a statistics acquisition module, operatively coupled to the one or more MACs, for compiling statistics on each of the plurality of MACs; and

a network processor, operatively coupled to the plurality of data link layer processors, for routing the one or more frames received from the plurality of data link layer processors.

3 (Original). The switching device of claim 2, wherein each of the data link layer processors further comprises one or more flow search engines for classifying the one or more frames based upon one or more properties associated with the frames.

4 (Original). The switching device of claim 3, wherein one or more properties comprise a source port, a VLAN tag state, a VLAN identifier, and a VLAN tag control information (TCI) field.

5 (Original). The switching device of claim 3, wherein the one or more flow search engines comprise one or more content addressable memories (CAMs).

6 (Original). The switching device of claim 5, wherein the one or more CAMs associated with each of the plurality of data link layer processors consists of QoS rules pertaining to the associated plurality of physical layer interfaces.

7 (Original). The switching device of claim 2, wherein data link layer processors are media access controller (MAC) processors.

8 (Original). The switching device of claim 2, wherein the switching device is selected from the group consisting of: a router, a multi-layer switching device, and a switch blade.

9 (Original). The switching device of claim 2, wherein the statistics compiled by the statistics acquisition module comprise ingress frame statistics.

10 (Original). The switching device of claim 9, wherein the ingress frame statistics are compiled as a function of VLAN entry.

11 (Original). The switching device of claim 10, wherein the ingress frame statistics compiled as a function of VLAN entry comprise:

the number of bytes enqueued at the data link layer processor;
the number of frames enqueued at the data link layer processor;
the number of non-unicast bytes enqueued at the data link layer processor; and
the number of non-unicast frames enqueued at the data link layer processor.

12 (Original). The switching device of claim 2, wherein the statistics compiled by the statistics acquisition module comprise egress frame statistics.

13 (Original). The switching device of claim 12, wherein egress frame statistics are compiled as a function of physical layer interface.

14 (Original). The switching device of claim 13, wherein egress frame statistics are further compiled as a function of VLAN entry.

15 (New). The switching device of claim 2, wherein said MAC preprocessor includes at least one of a traffic policer, a MAC buffer, a VLAN push module, a rate buffer, and an ingress bus transmitter.

16. (New). The switching device of claim 2, wherein said MAC postprocessor includes at least one of an egress bus receiver, a rate buffer, and a VLAN pop module.